Space Charge Limited Flow in the Gate Current of AlGaN/GaN HEMTs

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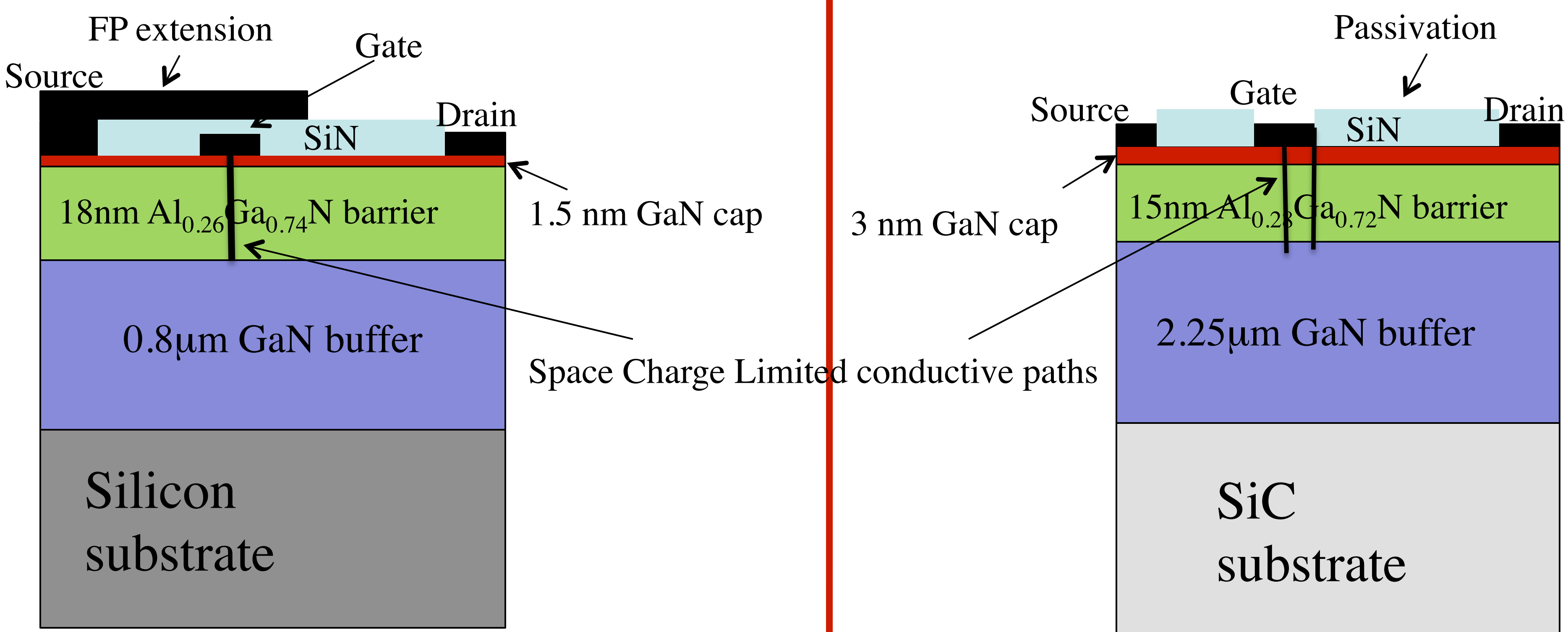
Outline

- AlGaN/GaN HEMT Devices under Study
- Review of Trap Free Space Charge Limited (SCL) Flow in Gate Stack
- Review of SCL Flow in the presence of Traps
- Experimental Results
- Discussion and Conclusions
- Current Work

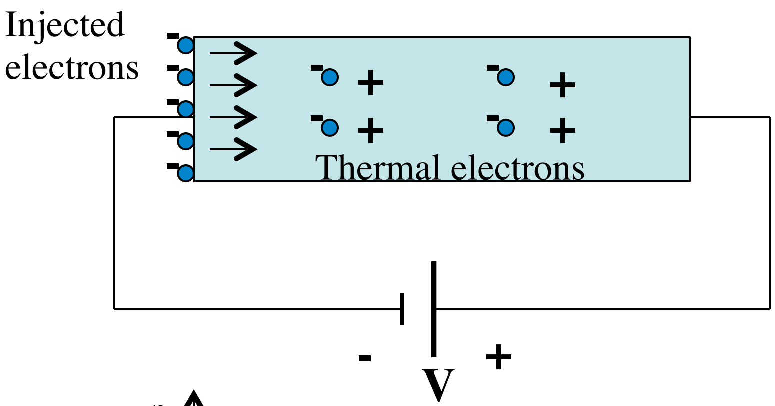
Devices under Study

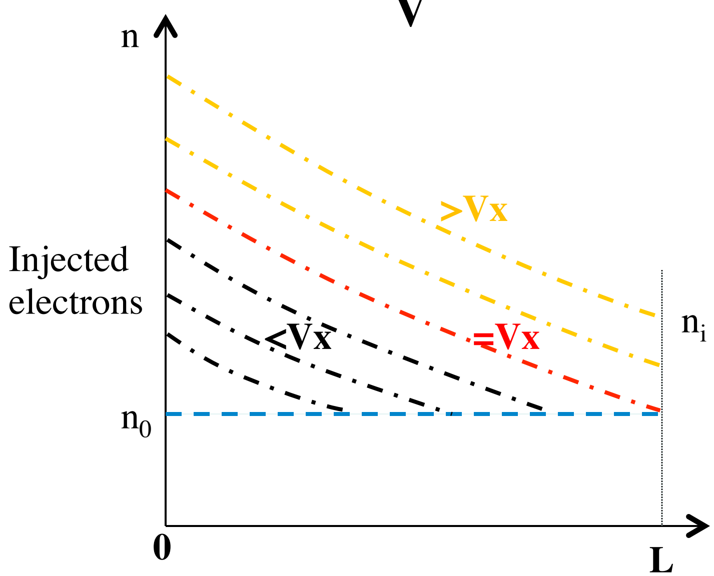


- Commercial device
- Gate length (L_G ~ 0.65 μm)
- 10 gate finger device with 2 mm periphery.
- Ceramic packaged.

- AFRL sample
- Gate length (L_G ~ 0.1 μm)
- 2 gate finger device with W_G ~ 160 μm
- Ceramic packaged.

Space Charge Carrier Injection





Transit time

$$t_{tr} = \frac{L}{V_d} = \frac{L^2}{\mu V} \qquad [1]$$

Dielectric relaxation time

$$t_{relax} = \rho\varepsilon = \frac{\varepsilon}{q n_0 \mu} \qquad [2]$$

When $t_{relax} = t_{tr}$

$$V_X = \frac{q n_0 L^2}{\varepsilon} \qquad [3]$$

The average injected excess free-electron density becomes comparable with n_0.

SCL of Trap-Free Case

Current ∝ Charge x Drift Velocity

As a function of applied voltage V

Charge

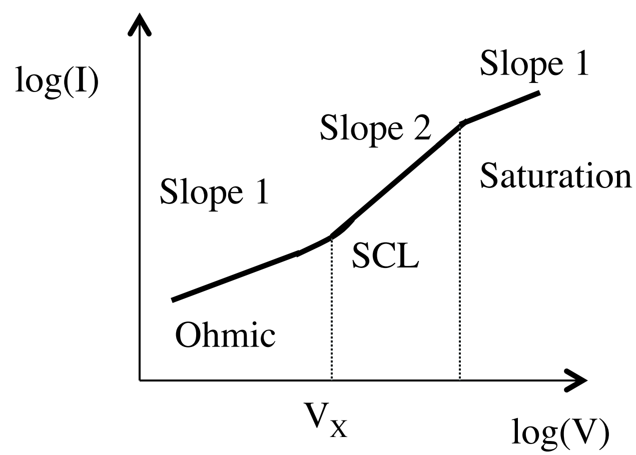
Constant from dopants, V^0 ↕ linear with injection via Q =C x V, V^1

Drift Velocity

At low field linear, V^1 ↔ high field saturation, V^0

Very distinctive electrical signature

First derived by M.A. Lampert, P. Mark, and J. C. Vesely



SCL Of Trap-Free Case

Start with Ohmic region

$$J = n_0 q v = n_0 q \mu \frac{V}{L} \quad [4] \qquad J \propto V$$

With increasing V, carriers accumulate, $Q = CV = \frac{\varepsilon}{L} V$ [5]

When injected carriers $\frac{Q}{L} > q n_0$

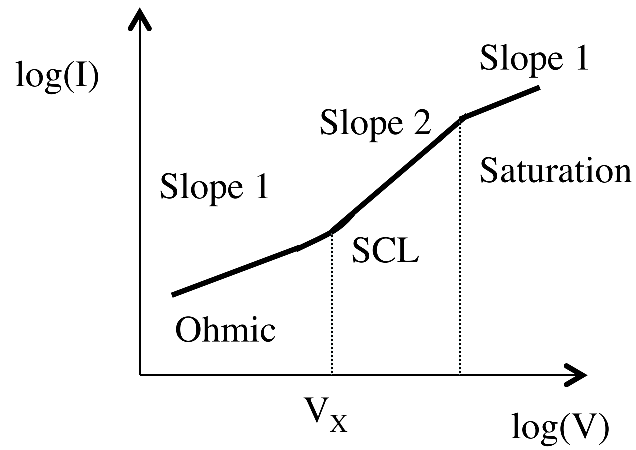
$$J = \frac{Q}{L} v = \varepsilon \mu \frac{V^2}{L^3} \quad [6] \qquad J \propto V^2$$

Keep increasing V until carriers' velocity saturates

$$J = \frac{Q}{L} v_{sat} = \varepsilon \frac{V}{L^2} v_{sat} \quad [7] \qquad J \propto V$$

Plot J vs V in log-log scale

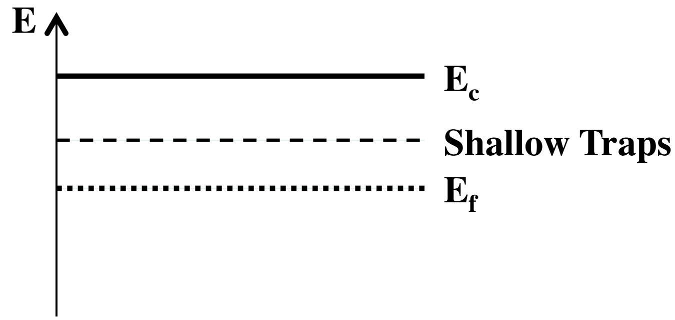
$$V_X = \frac{q n_0 L^2}{\varepsilon}$$



$$Q = (\rho + \rho_t)L = \frac{\varepsilon}{L}V$$

With shallow traps ($E_t >> E_f$)

$$\frac{n}{n_t} = \frac{\rho}{\rho_t} = \frac{N_c \exp[(E_t - E_c)/kT]}{gN_t} = \theta \qquad [8]$$



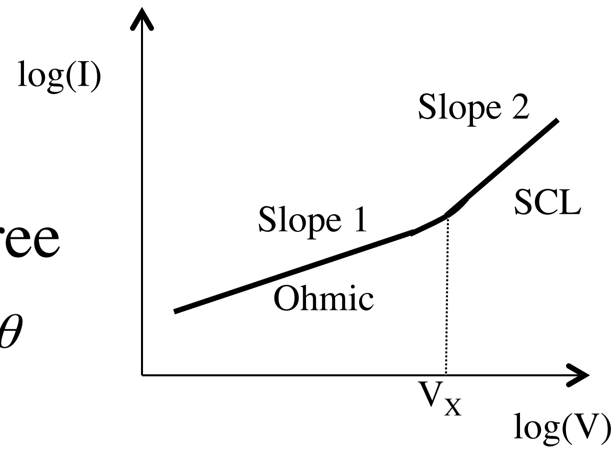
where θ is a constant (<<1) independent of injection level, as long as the traps remain shallow.

In SCL region

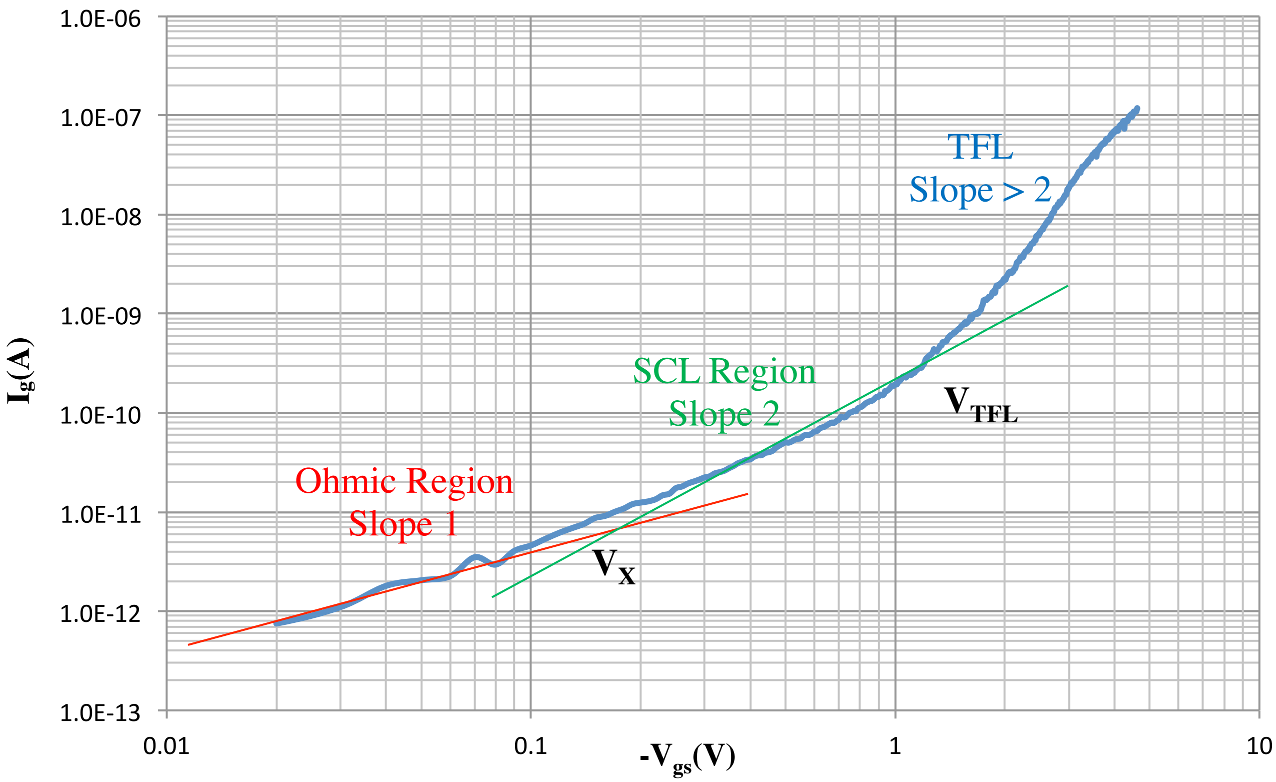
$$J = \theta\varepsilon\mu\frac{V^2}{L^3} \qquad [9]$$

The J-V plot is similar to the trap-free case except reducing by a factor of θ

$$V_X = \frac{qn_0L^2}{\theta\varepsilon} \qquad [10]$$



AFRL Virgin Devices

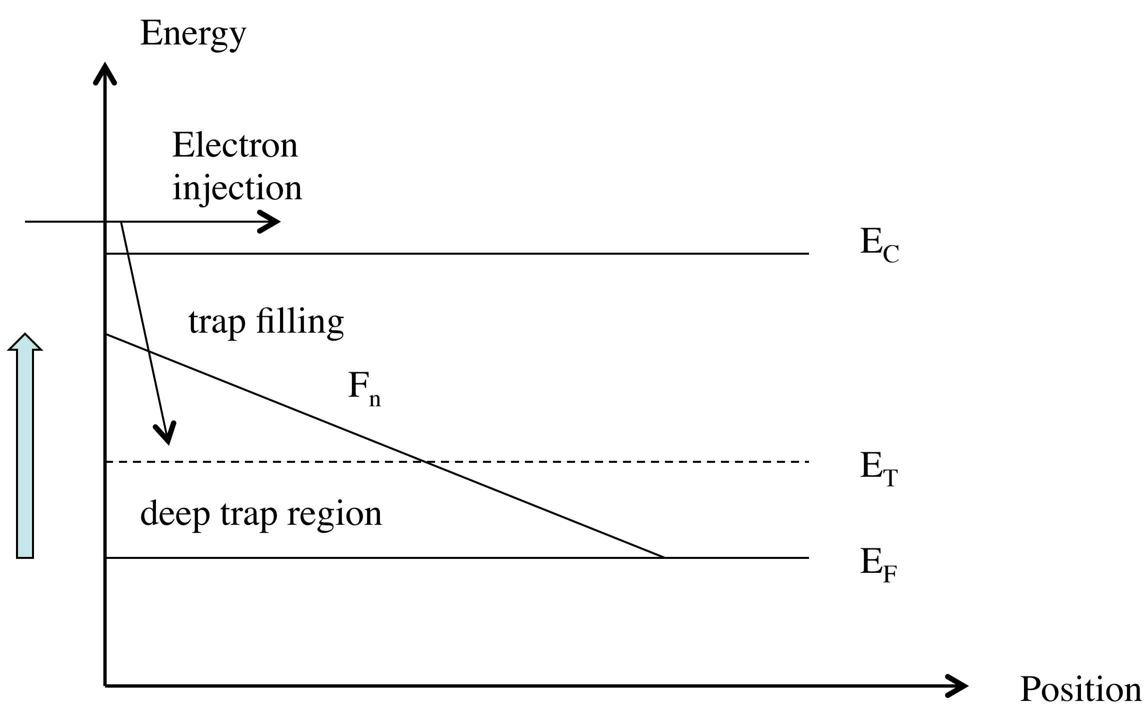


1223D gate leakage with shallow traps

V_X=0.18V V_{TFL}=1.1V

Quasi-Fermi level moves up with Injection

Energy band diagram versus position



SCL With Deep Traps

With deep traps ($E_t<E_f$)

The voltage required to fill the traps

$$V_{TFL}=\frac{qp_{t,0}L}{C}=\frac{qp_{t,0}L^2}{2\varepsilon} \qquad [11]$$

where $p_{t,0}$ is the hole occupancy of traps at equilibrium.

Since $J=qn\mu\frac{V}{L}$

Below V_{TFL}

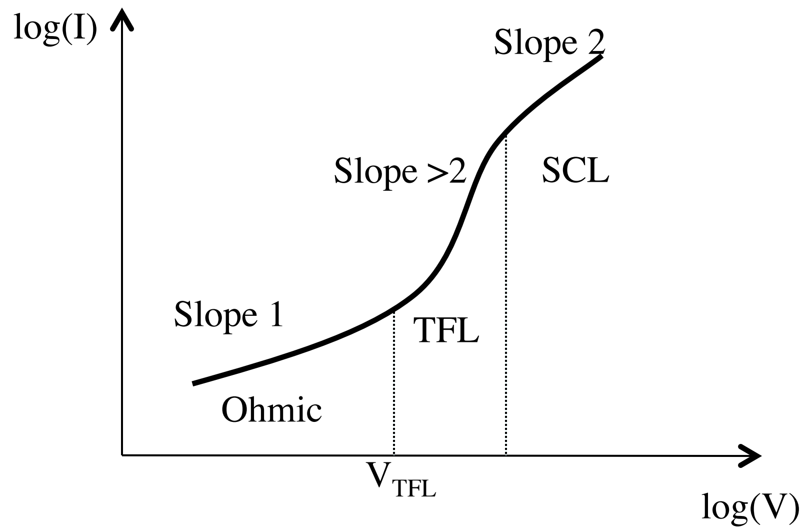
$$J=qn_0\mu\frac{V}{L}$$

At a voltage of $k.V_{TFL}$

$$n(k.V_{TFL})=(k-1)p_{t,0}$$

$$J(k.V_{TFL})=k(k-1)qp_{t,0}\mu\frac{V_{TFL}}{L} \qquad [12]$$

In J-V log plot a sudden rise at V_{TFL}



AFRL Virgin Devices

For 1223D $V_X = 0.18\text{V}$ $V_{TFL} = 1.1\text{V}$

$$V_X = \frac{qn_0L^2}{\theta\varepsilon} \qquad \theta = \frac{n_0}{n_{t,0}}$$

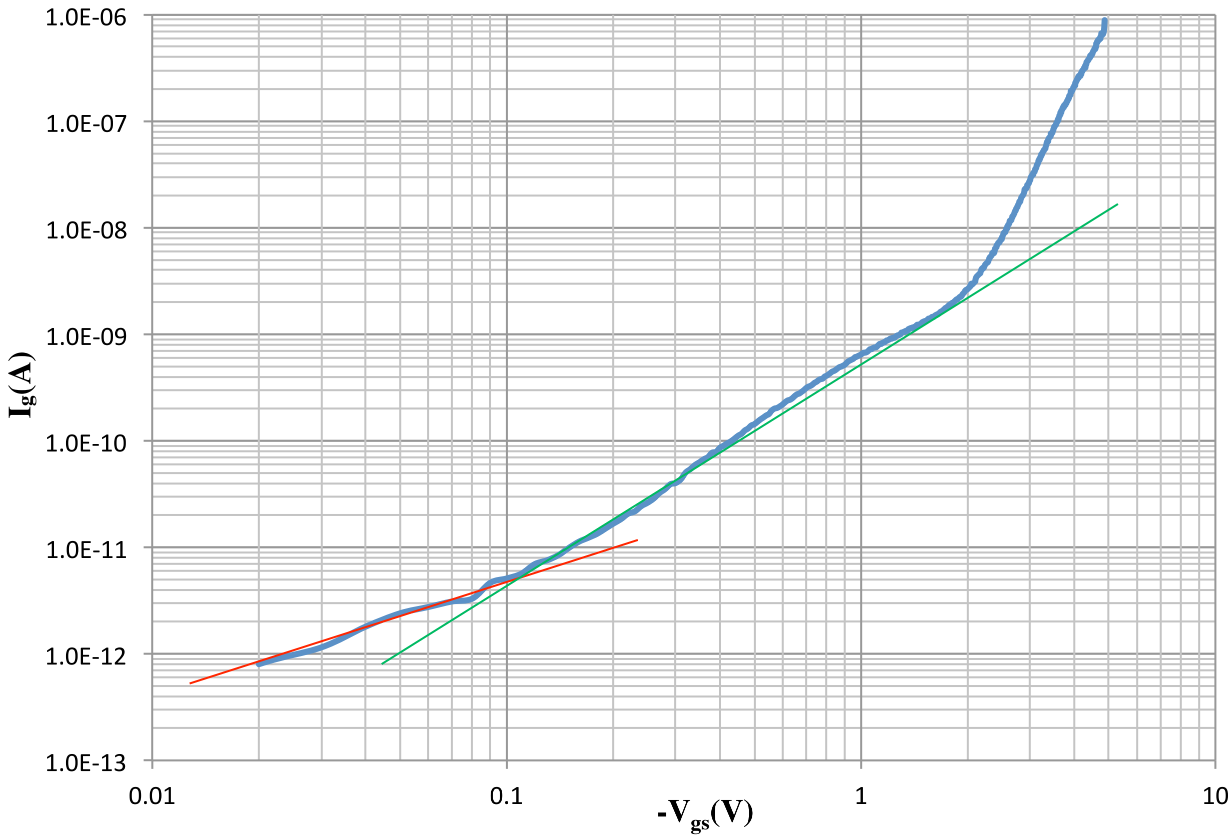
$$\mathrm{n}_{t,0} = \frac{n_0}{\theta} = \frac{\varepsilon V_{\mathrm{X}}}{qL^2} = 3.3\mathrm{x}10^{17}/cm^3$$

$$V_{TFL} = \frac{qp_{t,0}L^2}{2\varepsilon}$$

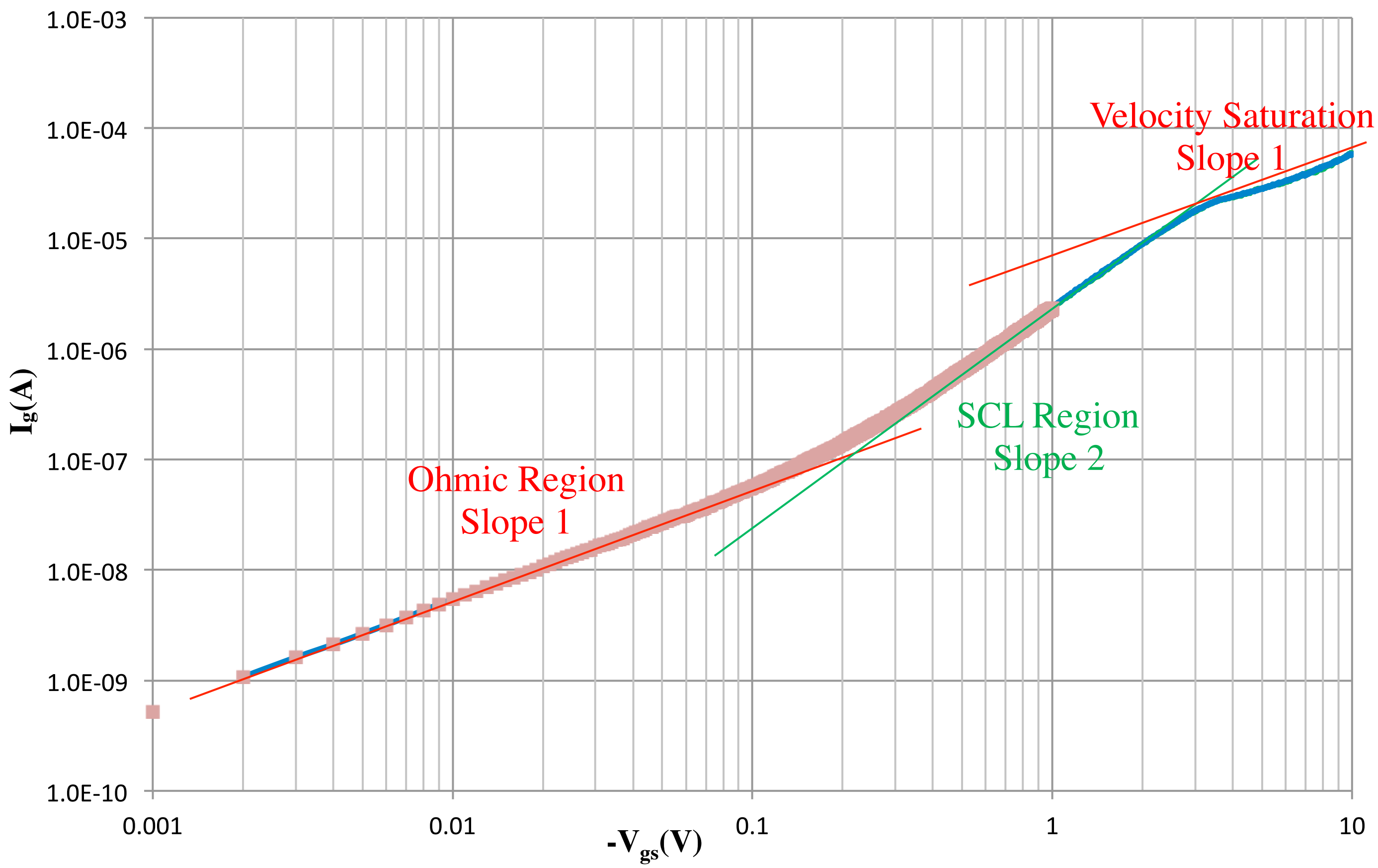
$$p_{t,0} = \frac{2\varepsilon V_{TFL}}{qL^2} = 2.9\mathrm{x}10^{18}/cm^3$$

$$\mathrm{N}_t = \mathrm{p}_{t,0} + \mathrm{n}_{t,0} = 3.3\mathrm{x}10^{18}/cm^3$$

AFRL Virgin Device



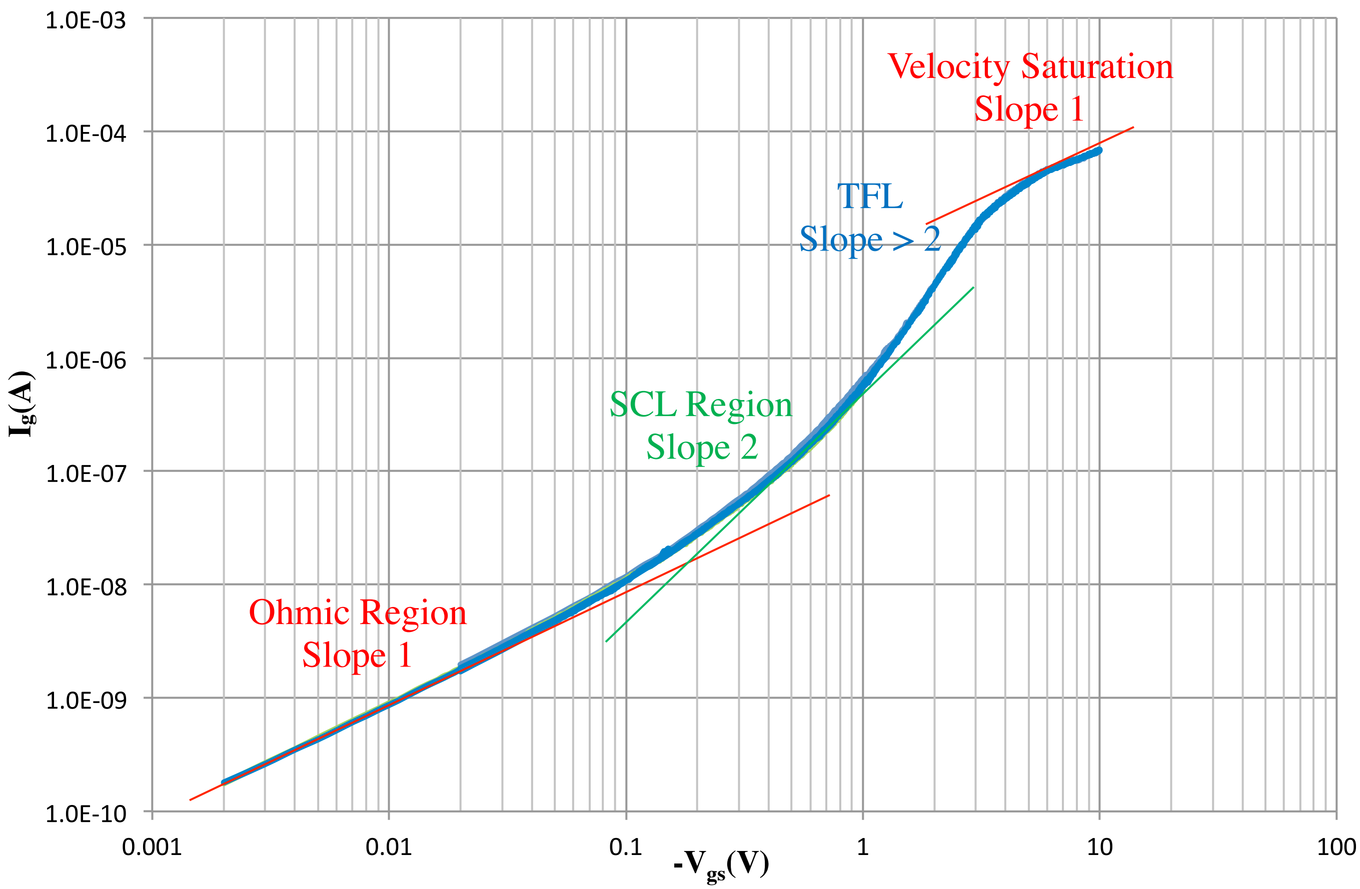
1624D gate leakage with shallow traps



1912C off-state stress from -10V to beyond critical voltage (-29V) with -1V/min increment for each step.

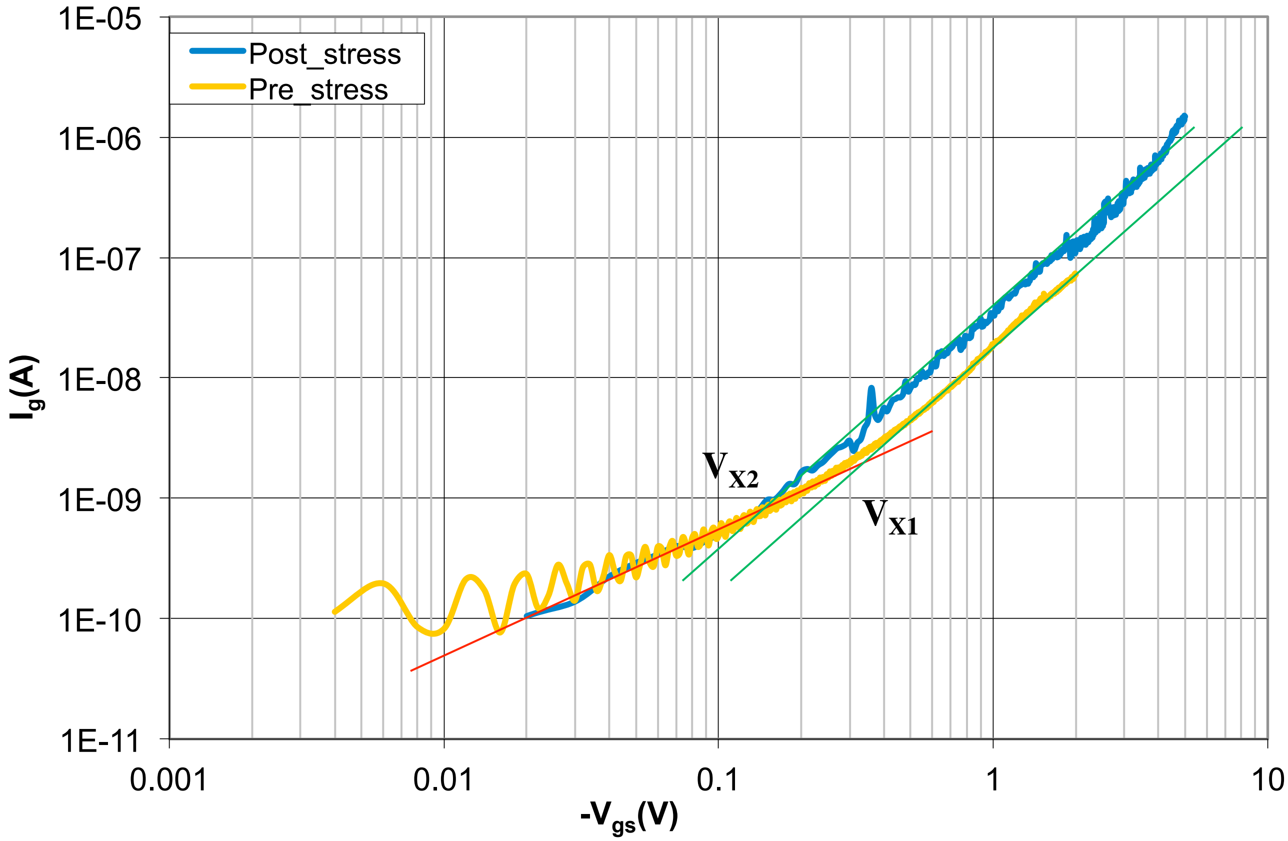
Shallow trap case with velocity saturation

AFRL Off-state Stress Device

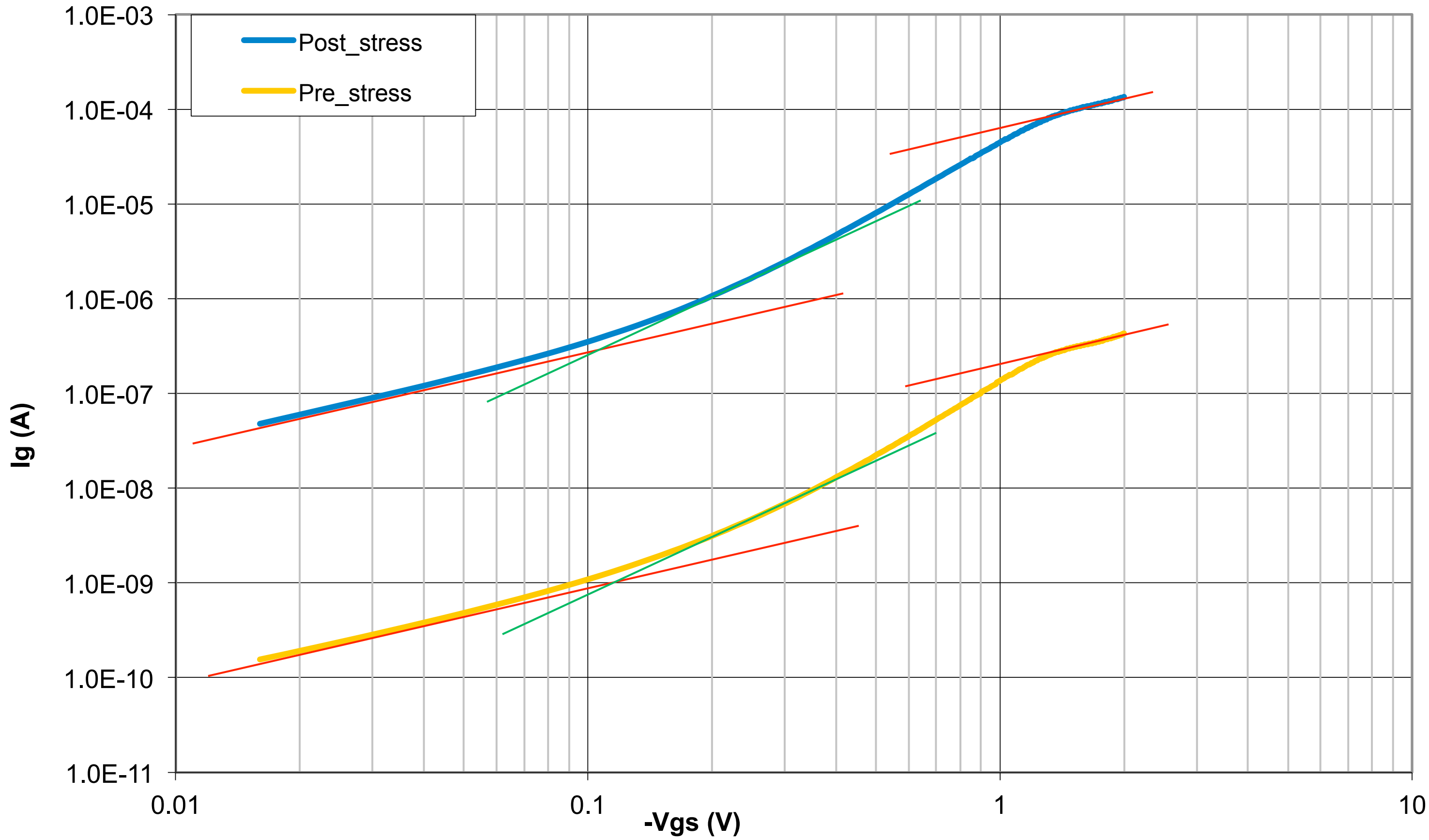


1812-23B off-state stress from -10V to beyond critical voltage (-22V) with -1V/min increment for each step. Shallow trap case with velocity saturation

Commercial Device



Device C1 through reverse gate voltage step-stress from -5V to -20V (much below the critical voltage) with -5V step size of 10 min each.



Device C2 was subjected to a forward gate voltage step stress from 1V to 3V with step size of 0.05V and 300s step duration time

Extracted Parameters

Device	Gate area	Stress Condition	Trap type	N_t (cm^{-3})	$p_{t,0}$ (cm^{-3})	$n_{t,0}$ (cm^{-3})	A_{eff} *(cm^2)
1912C	200μm*140nm*1	Reverse gate stress beyond critical voltage	Shallow			$3.2*10^{17}$	
1624D	200μm*170nm*2	Virgin	Shallow	$6.1*10^{18}$	$6.0*10^{18}$	$1.4*10^{17}$	
1812-23B	200μm*125nm*2	Reverse gate stress beyond critical voltage	Shallow	$3.0*10^{18}$	$2.7*10^{18}$	$2.7*10^{17}$	$1.9*10^{-12}$
1223D	200μm*170nm*2	Virgin	Shallow	$3.3*10^{18}$	$2.9*10^{18}$	$3.3*10^{17}$	
C1	0.5μm*200μm*10	Virgin	Shallow			$3.8*10^{17}$	
C1	0.5μm*200μm*10	Reverse gate stress below critical voltage	Shallow	$7.8*10^{18}$	$7.7*10^{18}$	$1.5*10^{17}$	
C2	0.5μm*200μm*10	Virgin	Shallow	$1.1*10^{18}$	$9.2*10^{18}$	$1.7*10^{17}$	$6.6*10^{-14}$
C2	0.5μm*200μm*10	Forward gate stress	Shallow	$1.0*10^{18}$	$8.2*10^{18}$	$1.5*10^{17}$	$2.2*10^{-11}$

Note that in some cases the extraction of data was limited by the number of domains that were observed.
A_{eff}*; the value of effective conduction area was calculated using $1.5*10^7$ cm/s as a number of saturation velocity in the conductive leakage path

Conclusions

- A_{eff} (10^{-14}-10^{-11} cm^2) is much smaller than the actual gate area of 10^{-7}-10^{-5} cm^2.
- SCL filaments are localized.
- IV curves of C2 before and after stress are in parallel and the parameters extracted are almost the same except for A_{eff}. This indicates that the increase in gate current is caused by merely an expansion of the leakage path area due to the stress applied.
- Velocity saturation observed among all stressed devices may indicate stress induced leakage path are more likely to happen at the gate edge where there is an electrical peak.

Current Work

- Studying devices which travelled from AFRL(?) to Ray Holzworth (Jones group).
- Gate current electrical signature consistent with SCL filament model.
- Developed and are currently testing a model to determine the lateral contact location of the SCL filaments with the source to drain channel.
- Studying the Random Telegraph gate current and noise resulting from the SCL filaments which may contain a very low number of electrons to unravel the transport mode (Variable Range Hopping?).

Questions?